Cambridge Assessment International Education

Cambridge IGCSE™

11: Electronics – Topic questions

Paper 4

The questions in this document have been compiled from a number of past papers, as indicated in the table below.

Use these questions to formatively assess your learners' understanding of this topic.

Question	Year	Series	Paper number
10	2016	June	41
11	2016	March	42
7	2016	November	42

The mark scheme for each question is provided at the end of the document.

You can find the complete question papers and the complete mark schemes (with additional notes where available) on the School Support Hub at www.cambridgeinternational.org/support

10 (a) (i) Fig. 10.1 shows the symbol for a circuit component.

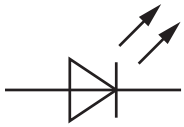


Fig. 10.1

Name this component.

..... [1]

(ii) In the space below, draw the symbol for a NOT gate.

[1]

(b) Fig. 10.2 shows a digital circuit.

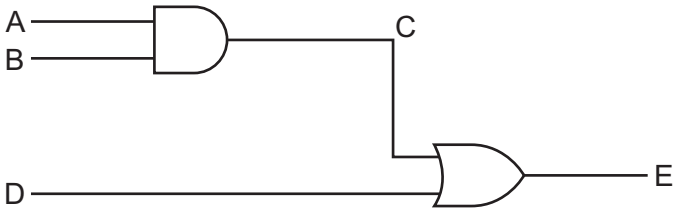


Fig. 10.2

Complete the truth table for this circuit.

input A	input B	output C	input D	output E
0	0		0	
0	0		1	
0	1		0	
0	1		1	
1	0		0	
1	0		1	
1	1		0	
1	1		1	

[3]

(c) Suggest a modification to the circuit in Fig. 10.2 to produce the output Z in the truth table below. It may help you to compare this truth table with the truth table in **(b)**.

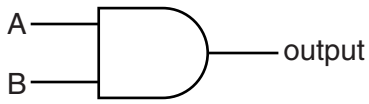
input A	input B	input D	output Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

.....

..... [1]

[Total: 6]

11 (a) (i) Fig. 11.1 shows the symbol for a logic gate and its truth table.

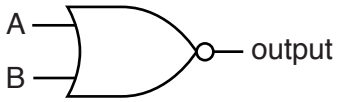


input A	input B	output
0	0	0
1	0	0
0	1	0
1	1	1

Fig. 11.1

State the name of this logic gate. .....[1]

(ii) Complete the truth table for the logic gate shown in Fig. 11.2.



input A	input B	output
0	0	
1	0	
0	1	
1	1	

Fig. 11.2

[2]

(b) Fig. 11.3 shows the system of logic gates used to ensure the security of the strongroom of a bank.

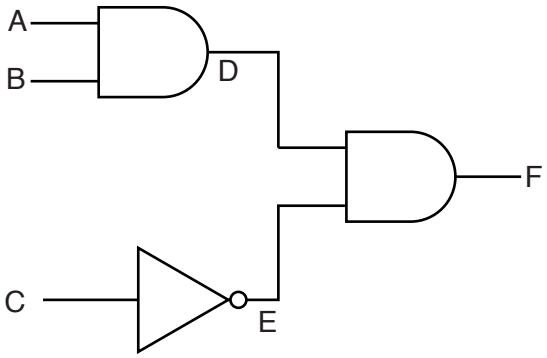


Fig. 11.3

The strongroom door will only open when the output F is logic 1.

Complete the table to show the logic states at A, B, C, D and E when the strongroom door can be opened.

input A	input B	input C	output D	output E	output F
					1

[3]

[Total: 6]

7 **(a)** In the space below, draw the circuit symbol for a thermistor.

[1]

(b) Fig. 7.1 shows the connections between two logic gates.

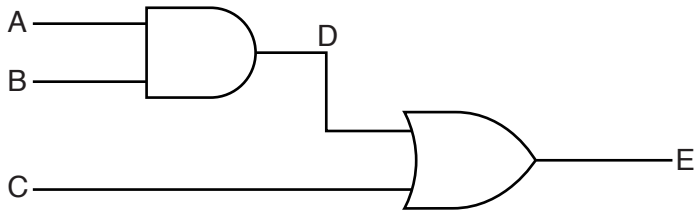


Fig. 7.1

Complete the truth table of this combination of logic gates.

inputs			intermediate point	output
A	B	C	D	E
0	1	1		
1	0	1		
1	1	0		
1	1	1		

[3]

(c) In the space below, draw a truth table to show the action of a NOT gate.

[2]

[Total: 6]

<table>
<tr><th>Question</th><th>Answer</th><th>Mark</th></tr>
<tr><td>10 (a) (i)</td><td>light emitting diode OR LED</td><td>B1</td></tr>
<tr><td>10 (a) (ii)</td><td>  </td><td>B1</td></tr>
<tr><td>10 (b)</td><td><table><tr><th>column C</th><th>column E</th></tr><tr><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td></tr></table></td><td>B3</td></tr>
<tr><td>10 (c)</td><td>replace the OR gate with an AND gate</td><td>B1</td></tr>
<tr><td></td><td></td><td>Total: 6</td></tr>
<tr><td>11 (a)</td><td>AND (gate)</td><td>B1</td></tr>
<tr><td>11 (b)</td><td>001
100
010
110</td><td>B2</td></tr>
<tr><td>11 (c)</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table></td><td>B3</td></tr>
<tr><td></td><td></td><td>Total: 6</td></tr>
<tr><td>7 (a)</td><td>  </td><td>B1</td></tr>
<tr><td>7 (b)</td><td>first 2 rows of D both 0
last 2 rows of D both 1
each row of column E logical OR of (column C and candidate’s column D)</td><td>B1
B1
B1</td></tr>
<tr><td>7 (c)</td><td>two single inputs 0 AND 1
two correct single outputs 1 AND 0</td><td>B1
B1</td></tr>
<tr><td></td><td></td><td>Total: 6</td></tr>
</table>

Notes about the mark scheme are available separately.